IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (currently amended): A method of manufacturing a semiconductor device, comprising ~~the steps of~~:

(a) forming a first interlayer insulation film on a semiconductor substrate;

(b) depositing ~~sequentially and patterning~~ a ~~predetermined~~ first metal film on said first interlayer insulation film; [[and]]

(c) depositing an antireflection film including a dielectric layer on ~~a semiconductor substrate~~ an upper surface of said first metal film ~~to form a lower electrode having said antireflection film on its upper surface~~;

(d) patterning said first metal film and said antireflection film to form a lower electrode having said antireflection film on an upper surface thereof; [[(b)]]

(e) forming [[an]] a second interlayer insulation film on said ~~lower electrode~~ antireflection film; [[and]]

(f) forming first and second openings ~~respectively~~ in a ~~capacitor element forming~~ first region [[of]] and in a ~~contact forming~~ second region [[of]] in said second interlayer insulation film, respectively ~~on said lower electrode~~; [[(c)]]

(g) removing a portion of said antireflection film [[in]] where said second opening is formed; ~~and (d)~~

(h) depositing a ~~predetermined~~ second metal film on said second interlayer insulation film; ~~having said first and second openings~~ and

(i) removing said second metal film ~~other than said second metal film~~ except in said first and second openings[[,]] to form an upper electrode ~~of said capacitor element~~ in said first opening, and a contact in said second opening.

Claim 2 (currently amended): The method of manufacturing a semiconductor device according to claim 1, further comprising ~~the step of~~: [[(e)]]

(j) depositing ~~and patterning~~ a ~~predetermined~~ third metal film on said second interlayer insulation film; and

(k) patterning said third metal film to form an interconnect line ~~which is~~ including a first portion and a second portion, said first and second portions of the interconnect line being individually connected to said contact and said upper electrode, respectively,

wherein said ~~step (e) being~~ steps (j) and (k) are performed after said step [[(d)]] (i).